Dkt. 2271/60617



Application of: Yoshinori UEDA

Serial No.: 09/431,593

Group Art Unit: 2815

Date Filed: November 1, 1999

Examiner: Matthew E. Warren

Mail Stop Issue Fee

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

For:

COMMUNICATION FORWARDING CORRECTED FORMAL DRAWINGS

SEMICONDUCTOR DEVICE HAVING AN INTEGRAL RESISTANCE ELEMENT

Applicant submits herewith Figs. 1 and 7 in connection with the above-identified application. The enclosed formal drawings are submitted in response to the Notice of Allowability dated November 12, 2004, in which the Examiner required Applicant to submit a new set of corrected drawings for Figs. 1 and 7 labeled as "replacement sheets". A response to the November 12, 2004 Notice of Allowability is due February 14, 2005. Accordingly, this Communication is being timely filed.

No fee is deemed necessary in connection with the filing of this Communication. However, if any fee is required, authorization is hereby given to charge the amount of such fee to Deposit Account No. 03-3125.

Respectfully submitted,

I hereby certify that this correspondence is being deposited this date with the U.S. Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Paul Teng Reg. No. 40,837 February 9, 20

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Paul Teng, Reg. No. 40,837

Attorney for Applicant Cooper & Dunham LLP

1185 Avenue of the Americas

New York, N.Y. 10036

(212) 278-0400